Remarks

All pending Claims 1 – 15 stand rejected by the Examiner under 35 U.S.C. §103(a). The references relied upon by Examiner to reject Claims 6-8, 11-13, and 16-18 under 35 U.S.C. §103(a) are U.S Patent 5,418,473 issued to *Canaris*, U.S. Patent 6,504,411 issued to *Cartegena*, and U.S. Patent 6,657,472 issued to *Raza et. al.* All pending claims deserve further consideration due to the clear differences between Applicant's invention and the teachings and suggestions of the prior art.

In response to the Office action, Applicant has canceled Claims 1-5, 7-10, and 11-15, has amended Claims 6 and 11 to particularly point out and distinctly claim the invention, and has added Claims 16-28 to more specifically claim a distinguishable invention. Claims 6, 11, and 16-28 now remain pending and are presented for further examination and consideration.

Requirements for *Prima Facie* Obviousness

The obligation of the examiner to go forward and produce reasoning and evidence in support of obviousness is clearly defined at M.P.E.P. §2142:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

M.P.E.P. §2143 sets out the three basic criteria that a patent examiner must satisfy to establish a *prima facie* case of obviousness:

1. some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;

2. a reasonable expectation of success; and

3. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

It follows that in the absence of such a *prima facie* showing of obviousness by the examiner (assuming there are no objections or other grounds for rejection), an applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443 (Fed. Cir. 1992).

Thus, in order to support an obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that each of the three aforementioned basic criteria has been met. The Applicant respectfully asserts that the rejection of Claims 6, and 11 herein fails under the all three prongs of the obviousness test because SEU flip-flops using the *Canaris* SEU NOR and SEU NAND circuits in combination with *Raza's* latches produces circuits that are quite different from Applicant's SEUSSNor and SEUSSNand circuits. Furthermore, *Cartegena's* circuit has multiple redundant elements none of which are SEUSSNor or SEUSSNand latches. It is impossible for *Cartegena* to teach or suggest the use of elements that were unavailable until disclosed by Applicant.

The prior art suggests two embodiments of an SEU latch wherein standard NAND based and NOR based flip-flops, as taught be *Raza*, are instantiated with the *Canaris* SEU NAND and SEU NOR circuits. As one skilled in the art, Examiner combined the teachings to develop SEU resistant flip-flops and stated that the combination was obvious. Applicant does not disagree, finding Examiners combination to be interesting because it can use fewer total gates than Applicant's invention if conjugate pairs of the input signals are already available. The prior art references, however, teach Examiner's combination while actually teaching away from Applicant's invention.

Applicant's invention is distinct from Examiner's combination in a

number of details. Most distinctively, Applicant's invention does not require conjugate pairs of input signals. For example, Applicant's Fig. 3 reveals single sided S and R inputs into Applicant's invention with conjugate pair Q and Q2 outputs. Examiner's combination requires SEU inverters at the inputs to obtain a similar property. Using the *Canaris* SEU inverters adds a total of eight more gates to Examiner's combination, resulting in at least 25% more gates than Applicant requires.

The only apparent motivation for adding SEU inverters to Examiner's combination is to duplicate Applicant's invention. Applicant's invention can not properly be used to teach the prior art. As such, the first prong of the test fails because Applicant's invention is distinct from and in most applications superior to Examiners combination and because the prior art does not contain some motivation or suggestion towards Applicant's invention. Rather, the prior art motivates and suggests towards Examiner's combination. Furthermore, *Cartegena's* self-redundant latch circuit uses components with single sided inputs and outputs. As such, combining *Raza* and *Canaris* produces an inferior circuit while combining that inferior circuit with *Cartegena* presents significant hurdles. The first prong certainly fails because Examiners combination would be difficult to instantiate and because, if instantiated, Examiners combination produces a redundant SEU circuit that is inferior to Applicant's.

Examiner relies on *Cartegena* to supply a prior art reference of a circuit using redundant latches, a voting sub circuit, and a feedback mechanism. The circuit of *Cartegena*, however, is quite distinguishable from Applicant's TRed1 and TRed2 circuits. *Cartegena* presents circuit details for a circuit with two redundant latches without examining the details involved in using three or more redundant latches. That, however, is an enablement problem for *Cartegena*. A more pertinent observation is the *Cartegena* requires the

individual latch outputs to be fed back while neither TRed1 nor TRed2 suffer from this limitation. As such, Applicant's circuits are distinguishable from and superior to *Cartegena's*.

The second prong of the test, a reasonable expectation of success, also fails. The only reasonable expectation is to produce a self redundant latch circuit with conjugate pair inputs as suggested by Examiner's combination. Applicant's circuit with its superior gate count would not result. An additional consideration is that using the *Canaris* gates in the *Cartegena* circuit would lead to failure because of the requirement for conjugate pair inputs.

The third prong fails because there is absolutely no teaching or suggestion in the prior art toward SEUSSNor or SEUSSNand circuits. Rather, the prior art teaches and suggests Examiner's combination which is demonstrably distinct. Furthermore, *Cartegena* does not suggest or teach that a new and superior circuit should be sought not does Furthermore, *Cartegena* does not suggest suggest what that circuit might be.

All three prongs of the test are required to support a *prima facie* case of obviousness. As such, the failure of only one prong is sufficient to establish Applicant's right to a patent. Here, all three prongs fail.

Conclusion

In view of the foregoing remarks, the Applicant submits that all pending claims are patentably distinct over the references and are in allowable form. Accordingly, the Applicant earnestly solicits the favorable consideration of the application, and respectfully requests that it be passed to issue in its present condition.

Should the Examiner discern any remaining impediment to the prompt

allowance of the aforementioned claims that might be resolved or overcome with the aid a telephone conference, he is cordially invited to call the undersigned at the telephone number set out below.

Respectfully submitted,

Richard H. Krukar
Attorney for the Applicant
Registration No. 53,162

Telephone No.: (505) 314-1270
Fax No.: (505) 314-1307

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